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REMARKS

Claims 1-9 are pending in the application. Applicants amend claims 1, 6, and 9 for clarification, and refer to Figs. 1 and 2 and their corresponding description in the specification for exemplary embodiments of and support for the claimed invention. No new matter has been added.

Claims 1-9 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Applicants' Admitted Prior Art ("AAPA") in view of U.S. Patent No. 6,662,216 to Lin. Applicants amend claims 1, 6, and 9 in a good faith effort to clarify the invention as distinguished from the cited references. Applicants respectfully traverse the rejection.

The Examiner asserted that AAPA discloses all aspects of the claimed invention except for the features of the claimed access controller of each processor. The Examiner relied upon Lin as a combining reference that allegedly teaches these features. In the Advisory Action, the Examiner continued to relied upon the description in Lin of having to invalidate (or replace) cached data when data in a slave device is changed as alleged disclosure of these features.

Again, Lin only includes a plain recognition that stale cached data needs to be replaced. And the cited portions of Lin only include description of "conventional logic" to monitor only "the write signal transferred on the control lines 250 to detect when information is to be changed within any of the slave devices 214 and 216 (Fig. 4)." Col. 5, lines 45-48 of Lin. If the data is cached, then the cache is "invalidated." Please see, e.g., col. 5, lines 65-66 of Lin.

Thus, even assuming, arguendo, that it would have been obvious to one skilled in the art at the time the claimed invention was made to combine AAPA and Lin, the combination would still have failed to disclose or suggest,

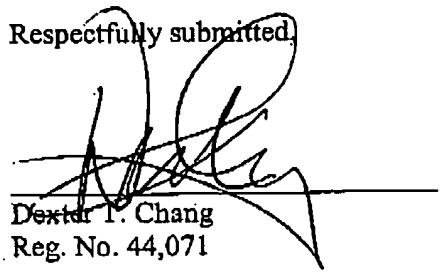
> "[a] multiprocessor system comprising a common memory and a number of processors connected via a common bus, only one processor being allowed to access same data area of said common memory at a time, wherein:
>
> said common memory is provided with a number of data areas that store data and with a control information area that stores control information indicating whether each of the data areas is in use;
>
> each processor is provided with a storage unit for storing same data and same control information as those stored in the common memory and with an access controller; and
>
> the access controller of a processor that does not have access privilege monitors data and addresses that flow on the common bus, accepts, from the common bus, ***data written to said common memory and data read from said common memory and stores this data in a memory area, which is designated by said address, of the storage unit within its own processor***," as recited in claim 1. (Emphasis added)

Accordingly, Applicants respectfully submit that claim 1, together with claims 2-5 dependent therefrom, is patentable over the cited references for at least the foregoing reasons. Claims 6 and 9 incorporate features that correspond to those of claim 1 cited above, and are, therefore, together with claims 7-8 dependent from claim 6, patentable over the cited references for at least the same reasons.

In view of the remarks set forth above, this application is in condition for allowance which action is respectfully requested. However, if for any reason the Examiner should consider this application not to be in condition for allowance, the Examiner is respectfully requested to telephone the undersigned attorney at the number listed below prior to issuing a further Action.

Any fee due with this paper may be charged to Deposit Account No. 50-1290.

Respectfully submitted,



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